Atty. Docket No. 55123P270
Express Mail Label No. EV387143785US

UNITED STATES PATENT APPLICATION

FOR

LOW TEMPERATURE COEFFICIENT INPUT OFFSET VOLTAGE TRIM WITH DIGITAL CONTROL

INVENTOR:
Simon Bevan Churchill

PREPARED BY:

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(714) 557-3800

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BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the field of bipolar differential amplifiers.

2. Prior Art

Input offset voltage trimming, both at wafer sort and final test, has been used in various guises for decades.

It has long been known that the best noise and offset performance is obtained from an input stage comprised of a resistively loaded long tailed pair followed by subsequent gain stages. Such a configuration is shown in outline in Figure 1. There are many ways to trim the input referred offset voltage but the preferred method is by modifying the current in R1 and R2. This can be accomplished, as shown, by changing the value of one of the load resistors, adding a compensating voltage or adding a compensating current. The correction circuitry needs to be implemented for both resistor loads as the error distribution is bipolar.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a diagram of a bipolar differential amplifier illustrating various ways of adjusting the input offset of the amplifier.

Figure 2 is a circuit diagram for a preferred embodiment of the present invention.

Figure 3 is a circuit diagram for an alternate embodiment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention provides a means of trimming the input offset voltage of an amplifier to approximately zero in a manner resulting in a low temperature coefficient of that offset voltage. The trim mechanism does not degrade inherent noise or offset parameters compared to an untrimmed amplifier. In addition, the trim can be performed under logic signal control, permitting post-package trimming or future recalibration after aging.

Justification for the preferred method of the present invention is given in the following analysis of factors that contribute to the input referred offset voltage. Note that the mismatch in Vbe between a matched pair of BJTs (bipolar junction transistors) is given by:

$$\Delta Vbe = V_T * ln\left(\frac{Ic1}{Ic2} * \frac{Area2}{Area1}\right)$$

where: V_T is the thermal voltage (KT/q)

Ic1 and Ic2 are the collector currents of transistors Q1 and Q2

Area1 and Area2 are the areas of transistors Q1 and Q2

Alternatively, Ic1/Area1 and Ic2/Area2 are the current densities in the transistors Q1 and Q2

The gain of a resistively loaded long tailed BJT pair is:

$$G = \frac{gm * Rc}{1 + gm * \frac{Rb'}{\beta} + gm * RE\left(\frac{1 + \beta}{\beta}\right)}$$

where: gm is the transconductance of each transistor

Rc is the collector load resistance

Rb' is the extrinsic base resistance

β is the current gain of each transistor

RE is the extrinsic emitter resistance

This gain is temperature independent if the tail bias current is set to ensure that:

$$Ic = \frac{G * V_T}{Rc - \frac{G * Rb'}{\beta} - \frac{G * (\beta + 1) * RE}{\beta}}$$

That is to say, a PTAT (proportional to absolute temperature) characteristic for transistors with large β and low extrinsic resistances.

Transistors Q1 and Q2

ΔVbe - the compensating current will restore the collector current densities to equality. The logarithmic term then becomes zero, and remains zero for all

temperatures. This is valid whether I_1 is PTAT or constant, if I_{ADJ} is a fixed proportion of I_1.

Resistors R1 and R2

ΔR - this is equivalent to an area mismatch in transistors Q1 and Q2 in that it causes a current density mismatch, and hence a ΔVbe in transistors Q1 and Q2, so the reasoning for ΔVbe is valid here also.

Transistors Q3 and Q4

ΔVbe - if the ratio of their collector currents (current densities) remains constant over temperature, then this error will be PTAT. Here again, this will be true, whether the tail current I_2 is PTAT or not. If the compensation current I_{ADJ} is also PTAT, then this error voltage can be directly compensated over temperature. While the ΔVbe of transistors Q1 and Q2 may be compensated whether the tail current I_1 is PTAT or not, simultaneous compensation of the ΔVbe of transistors Q3 and Q4 mandates that I_1 also have a PTAT characteristic if the compensation of both transistor pairs is to be accomplished by injection of an appropriate fraction of I_1 as a compensating current into the collector circuit of one of transistors Q1 and Q2.

$\Delta\beta$ - beta increases with temperature such that if the transistor is biased with a PTAT current, the resulting base current that is roughly constant over temperature would produce a corresponding offset voltage into resistors R1 and R2. If this voltage is compensated at room temperature by a PTAT I_{ADJ}, then over temperature the resultant PTAT error, divided by the first stage gain, will appear at the input.

If transistors Q3 and Q4 are biased with a constant current, then the resultant offset voltage into resistors R1 and R2 can be compensated roughly over temperature by a PTAT IADJ. Any resultant error is divided by the first stage gain before appearing as an input referred input offset voltage.

Transistors Q5 and Q6

ΔVbe - the mismatch voltage, when applied to resistors R3 and R4, produces a fixed PTAT current error on top of the intended bias current $I_2/2$. In order for the ratio of the collector currents to be temperature invariant, as required by transistors Q3 and Q4, current source I_2 must be PTAT. In this case, the ΔVbe is correctly compensated by I_{ADJ}.

Resistors R3 and R4

ΔR - this is equivalent to an area mismatch and hence a ΔVbe in Q5 and Q6, so that same reasoning as for ΔVbe is valid.

The circuit in Figure 1 is intended to help show the requirements for a circuit that exhibits low input offset voltage temperature drift after offset nulling, namely:

1. A symmetrical resistively loaded long tailed pair that is PTAT biased.

2. A symmetrical high gain second stage that is biased with a constant current if base current mismatch in transistors Q3 and Q4 dominates second stage input referred offset voltage contributions, else it is biased by a PTAT current.

This particular configuration does not allow the input common mode range to reach down to ground. However, it is relatively simple to reconfigure the second stage to enable a common mode range that includes ground without contravening the requirements or significantly degrading the efficacy of the solution. Similarly, other configurations using standard circuit techniques and optimized for alternative performance parameters can be devised without contravening the requirements.

There is a trend towards lower power circuitry, particularly as the level of integration increases. The value of I_{ADJ} is normally only a few percent of I_1. The trim range is normally split into 2^N steps, where N is the number

of digital control lines, to enable accurate input offset voltage nulling. Normally the generation of a small current in much smaller accurate increments requires very large device geometries and hence consumes an undesirable area of silicon. The present invention, as shown in Figure 2, provides an economical solution for low power circuits.

The circuit in Figure 2 is substituted for the collector loads R1 and R2 in Figure 1. The circuit comprises an R-2R ladder, represented by R_H and R_V, fed by N-1 identical switched current sources that are proportional replicas of I_1 in Figure 1. This forms a binarily scaled current divider that feeds the resultant current into load resistors R_T. The current can be shown to be equivalent to a compensation current, as shown in Figure 1, of:

$$I_{ADJ} = k * I_1 * \left(\frac{R_V}{R_V + R_T}\right) * \left(\frac{R_T}{R_T + R_C}\right) * \sum_{n=0}^{n=N-2} \frac{b_n * 2^n}{2^{N-2}}$$

where: b_N = 0 or 1, depending on the respective switch setting

Referring again to Figure 2, adding the compensation current I_{ADJ} to one of the trim resistors R_T does not change the effective load resistance of that leg, as the current sources kI_1 are high impedance sources. Instead, it is equivalent to adding an input offset adjustment voltage in

that leg of $V_{ADJ} = I_{ADJ}*R_T$. It is also equivalent to increasing the value of the respective resistor R_T so that the same current through the respective transistor will cause a higher voltage drop across the resistors making up its load.

For the binary scaling, it is necessary that $R_V = 2*R_H$, but there is no ratiometric constraint on R_T with respect to R_H. The crossover switch is controlled by the MSB and switches I_{ADJ} from one side to the other which enables compensation of bipolar distributions with only one network. The current source I_2 preferably is a constant current if base current mismatch in transistors Q3 and Q4 dominates second stage input referred offset voltage contributions, or alternatively is preferably biased by a PTAT current, typically proportional to I_1.

In Figure 2, typically the trim resistors R_T are a small percent of the primary load resistors R_C. Since the resistance looking into the R-2R ladder is R_V, a parallel resistance R_V is shown in the opposite leg to nominally balance the load resistance. Obviously, this resistance may be combined with the resistance of the associated trim resistor R_T as a single resistor. The crossover switch is a two pole, double throw transistor switch, allowing either leg

of the trim resistor network to be coupled to either leg of the transistor pair Q1 and Q2 - load resistors R_C, depending on the polarity of the initial input offset voltage.

As an alternative, the resistance R_V shown in parallel in the left leg of Figure 2 could instead have a higher resistance, or its resistance may be omitted. Since the effective resistance of the R-2R ladder is R_V, and the effect of the adjustment current is equivalent to increasing the value of the resistor R_T, the differential input stage will now nominally be biased for an input offset voltage of a fixed polarity, preferably slightly more than the maximum input offset expected. By proper selection of resistor ratios and other parameters, the range of input offset adjustment available may be set at twice the nominally biased input offset. Now the full expected range of input offset may be compensated by the adjustment current I_{ADJ} without requiring the crossover switch to control the polarity of the input offset as seen by the trim resistors R_T. One more bit in the R-2R ladder would be needed to obtain the same minimum increment in adjustability, though no more bits overall would be needed for the adjustment because of the elimination of the crossover switch and its control. Since both a ΔVbe in transistors Q1 and Q2 and a load resistor imbalance are compensated for by a PTAT I_{ADJ}, this compensation of the

offset of the differential input stage is also good with temperature variations.

Referring again to Figure 2, it may be seen that any one or more kI_2 current sources may be switched into a respective node of the R-2R ladder, or coupled to ground. The either/or coupling is preferred over an open circuit, as it provides a fixed load on the current sources, independent of their switch settings. As a further alternative, however, the R_V resistance in the left leg of Figure 2 may be eliminated, and in its place and as a replacement for the "or coupled to ground" connections, a second R-2R ladder could be provided (see Figure 3). Now any I_{ADJ} current source component may be coupled into either leg, allowing input offset voltage adjustment of either polarity and again eliminating the need for the crossover switch. Again, the crossover switch control bit may be used instead as an additional control bit for one bit longer R-2R ladders. Also now, each current source has twice the effect, though the additional (lower order) bit in the R-2R ladders makes up for this difference.

In all of the foregoing embodiments, the control of the crossover switch and/or the switches controlling the binary increments of the compensation current I_{ADJ} may be the same. Preferably a simple serial interface is used to set a nonvolatile register (see Figure 2) for storing one control

bit for each switch. In this way, amplifier input offset compensation may be done after packaging to also compensate for packaging stresses, and/or may be done after aging, or as often in use as the user desires, typically but not necessarily under software control. The serial interface minimizes pin count, as the present invention amplifiers are normally realized in integrated circuit form as one or more such amplifiers on a single integrated circuit, alone or with other circuitry. Other interfaces, or permanent compensation setting by blowing fuses, etc. could be used, though are not preferred.

While certain preferred embodiments of the present invention have been disclosed herein, such disclosure is only for purposes of understanding the exemplary embodiments and not by way of limitation of the invention. It will be obvious to those skilled in the art that various changes in form and detail may be made in the invention without departing from the spirit and scope of the invention as set out in the full scope of the following claims.